AMENDMENTS TO THE SPECIFICATION

Please delete the section entitled "SUMMARY OF THE INVENTION" in its entirety and substitute the following section therefor:

SUMMARY OF THE INVENTION

The present invention provides a scalable and configurable coprocessor interface that distinguishes between instruction types that are transferred between a central processing unit (CPU) and a coprocessor. The configurable coprocessor interface also allows sequential or parallel transfer of differing instruction types to one or more coprocessor pipelines. In addition, the interface provides separate TO/FROM data buses between the CPU and the coprocessor to allow for simultaneous data transfer (in/out) between the CPU and the coprocessor. Furthermore, the interface provides for disassociation between instructions that are transferred, and data that is transferred, to allow data elements to be moved in variable time slots with respect to their associated instructions. Moreover, the interface allows for out-of-order data elements to be transferred between the CPU and its coprocessors in an order that is not tied to the order that associated instructions are transferred (i.e., out-of-order data transfer). Out-of-order data transfer according to the present invention does not require order tags to be associated with each data transfer. Rather, the interface keeps track of the relative order of outstanding instructions that require data for execution, and provides a relative order indicator along with each piece of data as it is transferred. In addition, condition code signaling is provided from the coprocessor to allow the coprocessor to evaluate CPU specific conditional instructions, and to inform the CPU as to whether or not it should execute the CPU conditional instructions.

An embodiment of the present invention provides an interface for transferring data between a central processing unit (CPU) and a plurality of coprocessors. The interface includes an instruction bus and a data bus. The instruction bus transfers instructions to the plurality of coprocessors in an instruction transfer order, where particular instructions ~~direct designated ones~~ designate and direct one of the plurality of coprocessors to transfer the data to/from the CPU. The data bus is coupled to the instruction bus. The data bus

subsequently transfers the data, where data order signals within the data bus prescribe a data transfer order that differs from the instruction transfer order, and where the data order signals prescribe transfer of a data element. The data element corresponds to a specific outstanding instruction, where the data order is relative to outstanding instructions, the outstanding instructions being those of the particular instructions transferred to the one of the plurality of coprocessors that have not completed a data transfer. The interface keeps track of said data order, and where said data order signals indicate said data order, and where said data order signals are provided with said data element as said data element is transferred.

In another aspect, the present invention provides a computer program product for use with a computing device, the computer program product has a computer usable medium that includes computer readable program code embodied thereon. The computer readable program code, when used with the computing device, causes enablement of functions corresponding to a ~~causes a~~ coprocessor interface ~~to be described~~ that transfers data between CPU and a plurality of coprocessors. The computer readable program code has first program code and second program code. The first program code causes enablement of functions corresponding to ~~provides~~ an instruction bus, where the instruction bus is configured to transfer instructions to the plurality of coprocessors in an instruction transfer order, and where particular instructions direct designated ones of the plurality of coprocessors to transfer the data to/from the CPU. The second program code causes enablement of functions corresponding to ~~provides a~~ data bus. The data bus is configured to subsequently transfer the data, where data order signals within the data bus prescribe a data transfer order that is different from the instruction transfer order, and where the data order signals prescribe transfer of a data element. The data element corresponds to a specific outstanding instruction. The data order is relative to outstanding instructions. The outstanding instructions are those of the particular instructions transferred to the one of said plurality of coprocessors that have not completed a data transfer. The coprocessor interface keeps track of the data order, where the data order signals indicate the data order, and where the data order signals are provided with the data element as the data element is transferred.

In a further aspect, the present invention provides a an apparatus for transmitting program code. The apparatus includes a communication network having a transmission medium, for embodying a computer data signal therein. The computer data signal has computer-readable first program code and computer-readable second program code. The computer-readable first program code is for use with a computing device, where the computer-readable first program code, when used with the computing device, causes enablement of functions corresponding to ~~provides~~ an instruction bus for transferring instructions to a plurality of coprocessors in an instruction transfer order, where particular instructions direct particular coprocessors to transfer data to/from a CPU. The computer-readable second program code is for use with the computing device, where the computer-readable second program code, when used with the computing device, causes enablement of functions corresponding to ~~provides~~ a data bus for subsequently transferring the data, where data order signals within the data bus prescribe a data transfer order that differs from the instruction transfer order, and where the data order signals prescribe transfer of a data element. The data element corresponds to a specific outstanding instruction. The data transfer order is relative to outstanding instructions. The outstanding instructions are those of the particular instructions transferred to the particular coprocessor that have not completed a data transfer.

In yet another aspect, the present invention provides a method for transferring data between a CPU and a plurality of coprocessors. The method includes transmitting instructions to the plurality coprocessors, each of the instructions designating the one of the plurality of coprocessors, and each of the instructions directing a data transfer between the CPU and a specific coprocessor, where the transmitting is provided in a specific instruction order; and subsequently transferring the data in an order different from the specific instruction order. The transferring includes specifying transfer of a data element corresponding to a specific outstanding instruction, where the order of said transferring is relative to outstanding instructions, the outstanding instructions being those of the instructions transmitted to the one of the plurality of coprocessors that have not completed a data transfer; and providing the data order signals with the data element as the data element is transferred.

Other features and advantages of the present invention will become apparent upon study of the remaining portions of the specification and drawings.